EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	233	703/20.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 13:35
L2	45	ebiu	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 13:52
L3	100	(bus adj interface adj unit) and soc and test$3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:10
L4	47	L3 and verif$7	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:11
L5	25	L4 and @ad<"20020301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:11
L6	7	(bus adj interface adj module) and soc and test$3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:14

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9	65	soc and verif$7 and ((test adj bench) or testbench) and @ad<"20020301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:45

Results for "(ebiu) <and> (pyr >= 1913 <and> pyr <= 2002)"
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» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

1. **Core design and system-on-a-chip integration**
   Rincon, A.M.; Cherichetti, G.; Monzel, J.A.; Stauffer, D.R.; Trick, M.T.;
   Design & Test of Computers, IEEE
   Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):26 - 35
   Digital Object Identifier 10.1109/54.632878
   AbstractPlus | Full Text: PDF(228 KB) IEEE JNL
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2. **A Computer Vision and Robotics Laboratory**
   Jarvis, R.A.;
   Computer
   Volume 15, Issue 6, Jun 1982 Page(s):8 - 24
   AbstractPlus | Full Text: PDF(11232 KB) IEEE JNL
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3. **A Stability Criterion for Linear Networks Containing Time-Varying Capac**
   Sandberg, I.;
   Circuits and Systems, IEEE Transactions on [legacy, pre - 1988]
   Volume 12, Issue 1, Mar 1965 Page(s):2 - 11
   AbstractPlus | Full Text: PDF(984 KB) IEEE JNL
   Rights and Permissions

4. **Multirate and composite control of two-time-scale discrete-time systems**
   Litkouhi, B.; Khalil, H.;
   Automatic Control, IEEE Transactions on
   Volume 30, Issue 7, Jul 1985 Page(s):645 - 651
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5. **An overview of the COBRA-ABS high level synthesis system for multi-Fl**
   Duncan, A.A.; Hendry, D.C.; Gray, P.;
   FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposiu
   15-17 April 1998 Page(s):106 - 115
   Digital Object Identifier 10.1109/FPGA.1998.707888

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1. **C-based SoC design flow and EDA tools: an ASIC and system vendor pe**
Wakabayashi, K.; Okamoto, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
Volume 19, Issue 12, Dec. 2000 Page(s):1507 - 1522
Digital Object Identifier 10.1109/43.898829
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2. **Constraint driven pin mapping for concurrent SOC testing**
Yu Huang; Nilanjan Mukherjee; Chien-Chung Tsai; Samman, O.; Yahya Zaid
Tung Cheng; Reddy, S.M.;
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th A
the 15th International Conference on VLSI Design. Proceedings.
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3. **RF-SoC-expectations and required conditions**
Matsuzawa, A.;
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4. **A battery management system for stand-alone photovoltaic energy syst**
Duryea, S.; Islam, S.; Lawrance, W.;
Industry Applications Magazine, IEEE
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Digital Object Identifier 10.1109/2943.922452
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Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactio
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2. **An industrial view of electronic design automation**
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3. **System architecture for multi-technology testbench-on-a-chip**
Hodge, A.; Newcomb, R.; Zaghloul, M.; Tigli, O.;
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Volume 2, 26-29 May 2002 Page(s):II-736 - II-739 vol.2
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4. **C-based SoC design flow and EDA tools: an ASIC and system vendor pe**
Wakabayashi, K.; Okamoto, T.;
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Nuts and Bolts of Core and **SoC Verification** ... 5. CONCLUSIONS The fundamental problem
that **SoC** and Core **verification** efforts deal with is design complexity. ...
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M Puig-Medina, G Ezer, P Konas - Proceedings of the Design Automation Conference (DAC2000), 2000 - doi.ieeecomputersociety.org
... Tradi- tional processor **verification** environments cannot be easily merged into an **SOC verification** environment. In contrast, the ...
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IP reuse creation for system-on-a-chip design - all 3 versions »
PJ Bricaud - Custom Integrated Circuits, 1999. Proceedings of the IEEE ..., 1999 - ieeexplore.ieee.org
... creation for **SoC** design will be separated into system-level specification, soft-hard macro creation and productization, **SoC** integration and **SoC verification**. ...
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M Birnbaum, H Sachs - Computer, 1999 - ieeexplore.ieee.org
... Bus VCI and transaction specifications Implementation/**Verification** Phase 3: functional models for soft and hard virtual components, **SOC verification**, and firm ...
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... to the HSMC, or SDRAM to SDRAM), between memory and an external peripheral attached
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AA Duncan, DC Hendry, P Gray - Proc. Field-Programmable Custom Computing Machines, April, 1998 - doi.ieeecomputersociety.org
... (**EBIU**) Data Only External Bus Interface Unit **...** on emerging "system-on-chip" (**SOC**) devices
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B Blaner, D Czenkusch, R Devins, S Stever - ASIC/**SOC** Conference, 2000. Proceedings 13th Annual IEEE ..., 2000 - ieeexplore.ieee.org
... to SDRAM), between memory and an external peripheral attached to the **EBIU**, or between ...
Almost all cores on the **SOC** have some form of power management, ranging ...
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Target directed completion for bus transactions
BC Drerup, RN Iachetta Jr - 2002 - freepatentsonline.com
... 1, **SOC** 100 further comprises a target directed completion device 103 for providing an enhanced bus transaction interface between **EBIU** device 120, processor ...
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... Thus, at the mesh point t = tn+l the value of uit is m bh m uit(t,+l) =
ah **EbiU**,,i + q E &i(',)uq,,i j=l j=l + Yo + au(s) ds + q ...
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